

CLAIMS

- 1 1. An integrated circuit, comprising:
2 an array of memory cells, the array configured as a NAND array in a plurality of
3 columns and rows of memory cells, the columns comprising one or more sets of memory
4 cells in series coupled to a bit line, and the rows comprising sets of memory cells having
5 their respective gate terminals coupled to a word line, memory cells in the array
6 respectively comprising a gate terminal, a first channel terminal, a second channel
7 terminal and a channel region between the first and second channel terminals, a charge
8 trapping structure over the channel region, a tunneling dielectric between the channel
9 region and the charge trapping structure, and a blocking dielectric between the charge
10 trapping structure and the gate terminal;
11 circuitry to program the memory cells in the array by E-field assisted tunneling
12 through the tunneling dielectric by applying a positive voltage to the gate terminal and a
13 low voltage or ground to the first and second channel terminals; and
14 circuitry to read data from the memory cells.
- 1 2. The integrated circuit of claim 1, wherein the tunneling dielectric has a barrier
2 height and thickness sufficient to prevent direct tunneling.
- 1 3. The integrated circuit of claim 1, wherein the tunneling dielectric has a silicon-
2 dioxide equivalent thickness between about 30 Angstroms and about 70 Angstroms.
- 1 4. The integrated circuit of claim 1, wherein the tunneling dielectric comprises
2 silicon dioxide, and has a thickness greater than 30 Angstroms.
- 1 5. The integrated circuit of claim 1, wherein the tunneling dielectric comprises
2 silicon dioxide, and has a thickness between about 30 Angstroms and about 70
3 Angstroms.

- 1 6. The integrated circuit of claim 1, wherein the positive voltage is about 15 Volts or
2 greater.
- 1 7. The integrated circuit of claim 1, wherein the E-field is about 15 Volts over 5
2 nanometers, or higher.
- 1 8. The integrated circuit of claim 1, wherein said array of memory cells is
2 configured as a read only memory.
- 1 9. The integrated circuit of claim 1, wherein memory cells in said array have a
2 negative threshold voltage prior to programming.
- 1 10. The integrated circuit of claim 1, wherein memory cells in said array of memory
2 cells are configured for one-time programming.
- 1 11. The integrated circuit of claim 1, including a static random access memory array,
2 and logic which accesses data stored in said array of memory cells and the static random
3 access memory array.
- 1 12. The integrated circuit of claim 1, including a static random access memory array,
2 and a processor which executes instructions, including instructions for access to data
3 stored in said array of memory cells, and stored in the static random access memory
4 array.
- 1 13. The integrated circuit of claim 1, including a static random access memory array,
2 and a processor which executes instructions, including instructions for access to data
3 stored in said array of memory cells, and stored in the static random access memory
4 array, and wherein said logic to program comprises instructions executed by the
5 processor.

1 14. The integrated circuit of claim 1, wherein the charge trapping structure comprises
2 silicon nitride.

1 15. The integrated circuit of claim 1, wherein the charge trapping structure comprises
2 one or more of alumina, HfOx, ZrOx, or other metal oxide material.

1 16. A read only memory cell, comprising:
2 a first channel terminal;
3 a second channel terminal spaced away from the first channel terminal by a
4 channel, and wherein the channel is configured to have a negative threshold prior to
5 programming;
6 a charge trapping structure;
7 a gate;
8 a blocking dielectric between the charge trapping structure and the gate; and
9 a tunnel dielectric between the channel and the charge trapping layer, wherein the
10 tunnel dielectric has a barrier height and thickness sufficient to prevent direct tunneling,
11 the memory cell adapted for one-time programming by applying a positive voltage to the
12 gate and a low voltage or ground to the first and second channel terminals, and adapted
13 for use as a read only memory.

1 17. An integrated circuit on a single substrate, comprising:
2 an array of memory cells configured as read only memory, the array configured as
3 a NAND array in a plurality of columns and rows of memory cells, the columns
4 comprising one or more sets of memory cells in series coupled to a bit line, and the rows
5 comprising sets of memory cells having their respective gate terminals coupled to a word
6 line, memory cells in the array respectively comprising a gate terminal, a first channel
7 terminal, a second channel terminal and a channel region between the first and second
8 channel terminals, a charge trapping structure over the channel region, a tunneling
9 dielectric between the channel region and the charge trapping structure, and a blocking
10 dielectric between the charge trapping structure and the gate terminal

11 a plurality of word lines in the array contacting the gates of memory cells in
12 respective rows in the array;
13 a plurality of bit lines in the array coupled to sets of memory cells along
14 respective columns in the array;
15 an address decoder coupled to the plurality of word lines and the plurality of bit
16 lines to address selected memory cells in the array;
17 logic, coupled to the plurality of word lines and the plurality of bit lines, to
18 program the memory cells in the array E-field assisted tunneling of electrons to the
19 charge trapping structure by applying a positive voltage to the gate terminal and a low
20 voltage or ground to the first and second channel terminals; and
21 sense circuitry, coupled to the plurality of bit lines, to sense threshold voltages in
22 selected memory cells in the array.

1 18. The integrated circuit of claim 17, wherein the tunneling dielectric has a silicon
2 dioxide equivalent thickness between about 30 Angstroms and about 70 Angstroms.

1 19. The integrated circuit of claim 17, wherein the tunneling dielectric comprises
2 silicon dioxide, and has a thickness greater than 30 Angstroms.

1 20. The integrated circuit of claim 17, wherein the tunneling dielectric comprises
2 silicon dioxide, and has a thickness between about 30 Angstroms and about 70
3 Angstroms.

1 21. The integrated circuit of claim 17, wherein the positive voltage is about 15 Volts
2 or greater.

1 22. The integrated circuit of claim 17, wherein the E-field is about 15 Volts over 5
2 nanometers, or higher.

1 23. The integrated circuit of claim 17, wherein memory cells in said array have a
2 negative threshold voltage prior to programming.

1 24. The integrated circuit of claim 17, wherein memory cells in said array of memory
2 cells are configured for one-time programming.

1 25. The integrated circuit of claim 17, including a static random access memory array,
2 and logic which accesses data stored in said array of memory cells and the static random
3 access memory array.

1 26. The integrated circuit of claim 17, including a static random access memory array,
2 and a processor which executes instructions, including instructions for access to data
3 stored in said array of memory cells, and stored in the static random access memory
4 array.

1 27. The integrated circuit of claim 17, including a static random access memory array,
2 and a processor which executes instructions, including instructions for access to data
3 stored in said array of memory cells, and stored in the static random access memory
4 array, and wherein said logic to program comprises instructions executed by the
5 processor.

1 28. The integrated circuit of claim 17, wherein the charge trapping structure
2 comprises a layer of silicon nitride.

1 29. The integrated circuit of claim 17, wherein the charge trapping structure
2 comprises one or more of silicon nitride, HfO₂, etc.